IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte SUZUKI

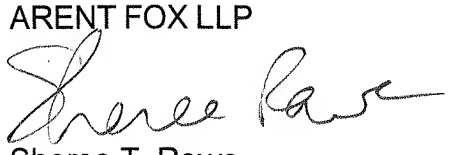
MOS TYPE IMAGE PICKUP DEVICE CAPABLE OF TAKING FULL PICTURE AT ONE TIME (as amended)

Application No.: 09/824,007
Filed: April 3, 2001
Appeal No.: Not Yet Assigned
Group Art Unit: 2622
Examiner: John M. VILLECCO

Submitted herewith is an Appeal Brief. The Commissioner is hereby authorized to charge any fee deficiencies required with respect to this paper, or credit any overpayment to Counsel's Deposit Account No. 01-2300, referencing Attorney Docket Number **107317-00026**.

Respectfully submitted,

ARENT FOX LLP



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Date: December 9, 2008

THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:

Nobuo SUZUKI

Group Art Unit: 2622

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BRIEF ON APPEAL

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I. INTRODUCTION

This is an appeal from the Final Office Action dated June 12, 2008, finally rejecting pending Claims 1, 4-8, 10-13 and 20 under 35 U.S.C. §103(a) as being unpatentable over Roberts (U.S. Patent No. 5,452,004, hereinafter "Roberts"). Claims 14-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest et al. (U.S. Patent No. 4,827,348, hereinafter "Ernest"). Claims 17-19 rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest, and further in view of Soeda et al. (U.S. Patent No. 5,382,974, hereinafter "Soeda"). The claim rejections were maintained in an advisory action dated October 24, 2008.

A Notice of Appeal was timely filed on November 12, 2008, with a two-month Petition for Extension of Time. Accordingly, the Appellant timely files this Appeal Brief.

II. REAL PARTY IN INTEREST

The real party in interest in the present application is Fujifilm Corporation, a corporation of Japan, as evidence by the assignment recorded at the United States Patent and Trademark Office on March 5, 2007, at Reel 018957, Frame 0495.

III. RELATED APPEALS AND INTERFERENCES

The Appellant, Appellant's legal representative, and assignee are not aware of any related appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

IV. STATUS OF CLAIMS

Claims 1, 4-8 and 10-20 are pending and rejected. Claims 1, 4-8 and 10-20 are being appealed. A copy of the claims under appeal is presented in Appendix I.

V. STATUS OF AMENDMENTS

The amendments submitted on August 21, 2007, in reply to the Final Office Action dated May 21, 2007, were entered in the Office Action dated September 4, 2007. The instant Appeal Brief is based upon the claims as finally rejected on June 12, 2008.

VI. SUMMARY OF THE CLAIMED SUBJECT MATTER

The claimed invention in claims 1, 4-8, and10-13 relates to an MOS-type solid-state image pickup device comprising: a semiconductor substrate (1); and a large number of pixels (10) arranged in one surface of said semiconductor substrate (1) in an array having a plurality of rows (shown with arrow 11) and a plurality of columns (shown with arrow 12). See Fig. 1A, page 12, line 25 - page 13, line 1. Each pixel (10) includes (a) a photoelectric converter element (20) having a cathode and (b) a switching circuit (SC) electrically connected to said cathode of the photoelectric converter element (20) for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode. See page 13, lines 2-5 and 21-25 and Fig. 1B.

The MOS-type solid-state image pickup device includes a plurality of row selection signal lines (27) disposed along a row direction, each being associated with one pixel row (shown with arrow 11) for supplying a row selection signal (see page 14, lines 25-26 and page 15, lines 13-16 and Fig. 1B); a plurality of output signal lines (30) disposed along a column direction, each being associated with at least one pixel column (shown with arrow 12) (see page 16, lines 2-4 and Fig. 1B); and a plurality of reset signal lines (28) disposed along the row direction, each being associated with one pixel row (shown by arrow 11) for supplying a reset signal (see page 15, lines 17-20 and Fig. 1B).

The MOS-type solid-state image pickup device also includes a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having

no random access function (see page 13, lines 6-20); a power source line (25); and an overall reset controller (47) for supplying an overall reset signal to all of said reset signal lines (28) at one time (see page 17, lines 7-8).

In the MOS-type solid-state image pickup device, the switching circuit (SC) includes a series connection of an output transistor (21) and a selection transistor (22) connected between the power source line (25) and an associated output signal line (30), the output transistor (21) having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor (22) having a gate connected to an associated row selection signal line; and a reset transistor (23) connected between said cathode and said power source line (25), and having a gate connected to an associated reset signal line. See page 13, lines 23-24 and page 14, line 17 – page 15, line 6.

The claimed invention in claims 14-19 relate to a digital camera including an MOS-type solid-state image pickup device similar to that in claim 1. The MOS-type solid state image pickup device in the digital camera of claim 14 further includes a readout row-shifter (43) for sequentially supplying the row selection signal to said row selection signal lines (27); a reset row-shifter (45) for sequentially supplying the reset signal to said reset signal lines (28); and an image signal outputting device (5) electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal. See page 13, lines 17-18 and page 16, line 25 – page 17, line 6.

The invention recited in claim 20 is directed to a MOS-type solid-state image pickup device similar to that in claim 1. In claim 20, the plurality of row selection signal lines (27) disposed along a row direction, each being associated with one pixel row for supplying a row selection signal are to select pixels of the associated pixel row, the plurality of output signal lines (30) disposed along a column direction, each being associated with at least one pixel column are for supplying output signals of the pixels selected by the row selection signal; and the plurality of reset signal lines (28) disposed along the row direction, each being associated with one pixel row are for supplying a

reset signal to clear the pixels of the associated pixel row. See page 15, lines 13-17 and page 16, lines 2-6.

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 4-8, 10-13 and 20 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts. Claims 14-16 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest. Claims 17-19 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest, and further in view of Soeda.

VIII. ARGUMENT

A. Legal Overview

To establish a *prima facie* case of obviousness, all of the claimed features must be taught or suggested by the references and there must be some suggestion or motivation, in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. See MPEP, section 2142.

B. The Cited Prior Art Fails to Teach or Suggest All Claim Elements

Claims 1, 4-8, 10-13 and 20 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts. Claims 14-16 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest. Claims 17-19 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over Roberts in view of Ernest, and further in view of Soeda.

Claim 1 is directed to an MOS-type solid-state image pickup device including at least a plurality of reset signal lines disposed along the row directions, each being associated with one pixel row for supplying a reset signal, in combination with the other elements recited in claim 1.

The reset signal lines are illustrated in the present application in Fig. 1 by lines 28 extending in the row direction.

The Appellant respectfully submits that the rejection is in error because the asserted combination of cited art fails to disclose or suggest at least this feature of claim 1.

In the Final Office Action dated June 12, 2008, the Examiner asserts that Roberts teaches a plurality of reset lines as "the traces 56 and 58 are used to send a logic signal to the FET (70) to connect the capacitor (44) to the trace 54 thereby resetting the pixel. See Office Action dated June 12, 2008 at page 2, second paragraph, lines 10-12.

In the response dated October 14, 2008, the Applicant replied that Roberts discloses only NOR gates 64, each connected with a row signal line 58 and a column signal line 56. The NOR gate 64 can supply an output in response to a combination of the row signal line and the column signal line. In Roberts, only when both signal lines 58 and 56 are LOW, the NOR gate 64 turns on transistor 70 to reset the capacitor 44. Thus, the row signal line 58 of Roberts does not constitute a reset signal line.

In the Advisory Action dated October 24, 2008, the Examiner asserts "that the address trace (58) can be interpreted to be the reset signal line, since it plays an active role in the resetting of the pixel. Even though the implementation of the reset function involves more than just trace (58), it still plays a role in the resetting of the pixel and therefore, can be interpreted to be a reset signal line."

The Appellant respectfully disagrees. Traces 56 and 58 supply signals to inputs 60 and 62 of NOR gate 64. Only when both the vertical traces 56 and the horizontal traces 58 supply a particular, combined selection signal, does the NOR gate 64 supply an output signal to transistor 70 which resets the storage capacitor 44. Without the column address traces 56, traces 58 cannot "reset" the storage capacitor. The output signal from the NOR gate 64 is more like "a" complete reset signal. In contrast, the signal sent along horizontal traces 58 is merely part of an input that can be combined

with a particular signal from vertical traces 56 in order to trigger a reset signal from NOR gate 64.

The Appellant notes that traces 56 and 58 extend vertically and horizontally, respectively. While the Appellant admits that rows and columns can be interchanged, if the vertical direction in Roberts is interpreted as the row direction, then the horizontal direction will be the column direction.

On page 5, paragraph 10, lines 11-12 of the Office Action dated June 12, 2008, the Examiner states that Roberts discloses "a plurality of row selection signal lines (Fig. 2, elements 56') disposed along a row direction, each being associated with one pixel row for supplying a row selection signal." If vertical elements 56 extend in a row direction, then horizontal elements 58 cannot also extend in a row direction.

Further, the Appellant notes that traces 56 extend along the vertical direction and are connected to transistors 76 that supply output signals of the storage capacitors 44 to output signal lines 78. The Examiner appears to interpret traces 56 to be "row" address lines and then also to be reset lines. These interpretations are contradictory. Furthermore, if traces 56 are "row" address lines, traces 58 cannot be "row" reset lines because they extend perpendicular to traces 56. Thus, traces 58 would extend in a "column" direction.

In claim 1, the "reset signal lines [are] disposed along the row direction, each being associated with one pixel row for supplying a reset signal." In claim 1, each reset signal line associated with one pixel row supplies the complete "reset signal" to that one pixel row. Thus, traces 58 are not reset signal lines "disposed along the row direction, each being associated with one pixel row for supplying a reset signal," as recited in claim 1

Ernest and Soeda fail to cure the deficiency in Roberts. Thus, even if combined (not admitted) Roberts, Ernest, and Soeda fail to disclose or suggest each element of claim 1.

Therefore, for at least the above noted reason, the Appellant submits that claim 1 is allowable over the cited art.

Independent claims 14 and 20 similarly contain "a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal" and "a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal to clear the pixels of the associated pixel row," respectively.

Thus, the Appellant submits that independent claims 14 and 20 are also allowable for at least the reasons described above for claim 1. As independent claims 1 and 14 are allowable, the Appellant submits that claims 4-8, 10-13, and 15-16, which depend from allowable claims 1 and 14, are therefore also allowable for at least the above noted reason and for the additional subject matter recited therein.

For at least the above reasons, the Appellant respectfully requests this Board to reverse the Examiner with respect to the rejection of Claims 1, 4-8, 10-16 and 20 under 35 U.S.C. §103(a) over Roberts.

C. The Examiner has Failed to Establish Prima Facie Obviousness

To establish a *prima facie* case of obviousness, all of the claimed features must be taught or suggested by the references. As noted above, the proposed combination of Roberts, Ernest, and Soeda, even if combined (not admitted) fail to disclose at least one element of claims 1, 4-8, 10-16 and 20. Accordingly, the Appellant respectfully submits that the Examiner has failed to set forth a *prima facie* case of obviousness with respect to Claims 1, 4-8 and 10-20.

IX. CONCLUSION

The Appellant respectfully submits that Claims 1, 4-8 and 10-20 are not unpatentable under 35 U.S.C. § 103(a) and respectfully requests the Honorable Board to reverse the rejections.

Respectfully submitted,

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X. APPENDIX I: COPY OF THE CLAIMS INVOLVED IN THE APPEAL

1. (Previously Presented) A MOS-type solid-state image pickup device comprising:

a semiconductor substrate;

a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal;

a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column;

a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal;

a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

a power source line; and

an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) A MOS-type solid-state image pickup device according to claim 1, further comprising:

an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal.

5. (Previously Presented) A MOS-type solid-state image pickup device according to claim 4, wherein said image signal outputting device comprises:

at least one analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal; and

a row-directional shifter for controlling operation of said analog signal generator and for sequentially outputting the analog voltage signal from said at least one analog signal generator.

6. (Previously Presented) A MOS-type solid-state image pickup device according to claim 4, wherein said image signal outputting device comprises:

an analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal;

an analog-to-digital converter for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and

a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom.

7. (Previously Presented) A MOS-type solid-state image pickup device according to claim 4, further comprising a controller for controlling operations of said overall reset controller, said row read scan circuit, said reset scan circuit, and said image signal outputting device.

8. (Previously Presented) A MOS-type solid-state image pickup device according to claim 1, further comprising:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor, said transfer transistor including a control terminal electrically connected to said transfer signal line.

9. (Canceled)

10. (Previously Presented) A MOS-type solid-state image pickup device according to claim 8, further comprising:

an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal.

11. (Previously Presented) A MOS-type solid-state image pickup device according to claim 10, wherein said image signal outputting device comprises:

at least one analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal; and

a row-directional shifter for controlling operation of said analog signal generator and for sequentially outputting the analog voltage signal from said analog signal generator.

12. (Previously Presented) A MOS-type solid-state image pickup device according to claim 10, wherein said image signal outputting device comprises:

an analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal;

an analog-to-digital converter for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and

a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom.

13. (Previously Presented) A MOS-type solid-state image pickup device according to claim 10, further comprising a controller for controlling operations of said overall reset controller, said row read scan circuit, said reset scan circuit, said transfer control row-shifter, and said image signal outputting device.

14. (Previously Presented) A digital camera, comprising:

a MOS-type solid-state image pickup device comprising:

(i) a semiconductor substrate;

(ii) a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

(iii) a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal;

(iv) a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column;

(v) a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal;

(vi) a readout row-shifter for sequentially supplying the row selection signal to said row selection signal lines;

(vii) a reset row-shifter for sequentially supplying the reset signal to said reset signal lines;

(viii) an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

(ix) a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

(x) an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal; and

(xi) a power source line;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge

accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line;

an image signal processor for generating mobile picture data or still picture data using the image signal outputted from said MOS-type solid-state image pickup device;

a light shielding device for interrupting light incident to said MOS-type solid-state image pickup device;

a still picture indication signal generator for generating a still picture indication signal indicating shooting of a still picture;

a mobile picture mode controller electrically connected to said MOS-type solid-state image pickup device for continually control operation thereof for repeatedly conducting (a) an image readout operation in which the row selection signal is sequentially supplied from said readout row-shifter to a predetermined number of row selection signal lines for sequentially outputting from said image signal outputting device an image signal representing the output signal generated on each said output signal line and (b) an electronic shutter operation in which the reset signal is sequentially supplied from said reset row-shifter to said reset signal supply lines at least associated with said pixel row as an object of the image signal readout operation for sequentially discharge electric charge accumulated in said photoelectric converter elements; and

a first still picture mode controller electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state

image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said reset row-shifter are stopped, and electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which said light shielding device is operated and interrupts the incident light for a predetermined period of time after the overall reset operation is finished, and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device.

15. (Previously Presented) A digital camera according to claim 14, wherein:

when an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, said first still picture mode controller does not interrupt the operation; and

when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, said first still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then the first still picture mode controller conducts the overall reset operation.

16. (Previously Presented) A digital camera according to claim 14, wherein said MOS-type solid-state image pickup device further comprises:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises

a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor,

said transfer transistor including a control terminal electrically connected to said transfer signal line

said mobile picture mode controller or said first still picture mode controller conducting said transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each said transfer signal lines associated with said pixel row as an object of the operation.

17. (Previously Presented) A digital camera according to claim 14, further comprising:

a strobe device for emitting flash light when a predetermined signal is received or said strobe device installing device for installing therein;

a second still picture mode controller electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said reset row-shifter are stopped, and

electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which after the overall reset operation is finished, a strobe device operation signal is generated for operating said strobe device; said light shielding device is operated and interrupts the incident light for a predetermined period of time after said strobe device operation signal is generated; and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device; and

a still picture mode specifying device for specifying, beforehand, a still picture mode controller to be operated when the still picture indication signal is outputted.

18. (Previously Presented) A digital camera according to claim 17, wherein:

when an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, said second still picture mode controller does not interrupt the operation; and

when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, said second still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then the second still picture mode controller conducts the overall reset operation.

19. (Previously Presented) A digital camera according to claim 17, wherein said MOS-type solid-state image pickup device further comprises:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises

a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor,

said transfer transistor including a control terminal electrically connected to said transfer signal line.

said mobile picture mode controller, said first still picture mode controller or said second still picture mode controller conducting said transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each said transfer signal lines associated with said pixel row as an object of the operation.

20. (Previously Presented) A MOS-type solid-state image pickup device comprising:

a semiconductor substrate;

a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal to select pixels of the associated pixel row;

a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column for supplying output signals of the pixels selected by the row selection signal;

a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal to clear the pixels of the associated pixel row;

a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

a power source line; and

an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line.

XI. APPENDIX II: EVIDENCE

-- NONE --

XII. APPENDIX III: RELATED PROCEEDINGS

-- NONE --